



IV Year-I Semester		T	P	C
		4	0	3

COMPUTER ARCHITECTURE AND ORGANIZATION(RT41044)

Prerequisite Course:

NIL

Course Description and Objectives:

The main objectives of this course are given below:

- Understand the fundamentals of different instruction set architectures and their relationship to the CPU design.
- Understand the principles and the implementation of computer arithmetic and ALU.
- Understand the memory system, I/O organization
- Understand the operation of modern CPUs including interfacing, pipelining, memory systems and busses.
- Understand the principles of operation of multiprocessor systems.

Course Outcomes:

Upon completion of the course, the student will be able to achieve the following outcomes.

Cos	CourseOutcomes	POs
1	Students can understand the architecture of modern computer.	3
2	They can analyze the Performance of a computer using performance equation	3
3	Understanding of different instruction types	4
4	Students can calculate the effective address of an operand by addressing modes	4

Syllabus:

UNIT I:

Objective: To Understand the principles and the implementation of computer arithmetic and ALU.

BASIC STRUCTURE OF COMPUTERS: Computer Types, Functional units, Basic operational concepts, Bus structures, Software, Performance, multiprocessors and multi computers. Data types, Complements, Data Representation. Fixed Point Representation. Floating – Point Representation. Error Detection codes.

COMPUTER ARITHMETIC: Addition and subtraction, multiplication Algorithms, Division Algorithms, Floating point Arithmetic operations. Decimal Arithmetic unit, Decimal Arithmetic operations.

UNIT II:

Objective: To Understand the fundamentals of different instruction set architectures and their relationship to the CPU design.

REGISTER TRANSFER LANGUAGE AND MICRO-OPERATIONS: Register Transfer language. Register Transfer, Bus and memory transfer, Arithmetic Micro-operations, logic micro operations, shift micro-operations, Arithmetic logic shift unit. Instruction codes. Computer Registers Computer instructions –Instruction cycle. Memory Reference Instructions. Input Output and Interrupt. **CENTRAL PROCESSING UNIT** - Stack organization. Instruction formats. Addressing modes. DATA Transfer and manipulation. Program control. Reduced Instruction set computer



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA

KAKINADA-533003, Andhra Pradesh, India

R-13 Syllabus for ECEJNTUK

UNIT III:

Objective: To Understand about Microprogrammed Control

MICRO PROGRAMMED CONTROL: Control memory, Address sequencing, micro program example, Design of control unit-Hard wired control. Micro programmed control

UNIT IV:

Objective: To Understand about various memory systems.

THE MEMORY SYSTEM: Memory Hierarchy, Main memory, Auxiliary memory, Associative memory, Cache memory, Virtual memory, Memory management hardware

UNIT V:

Objective: To Understand about different I/O organization.

INPUT-OUTPUT ORGANIZATION : Peripheral Devices, Input-Output Interface, Asynchronous data transfer Modes of Transfer, Priority Interrupt, Direct memory Access, Input –Output Processor (IOP), Serial communication;

UNIT VI:

Objective: Understand the operation of modern CPUs including interfacing, pipelining, memory systems and busses.

PIPELINE AND VECTOR PROCESSING: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline Vector Processing, Array Processors. **Multi processors:** Characteristics of Multiprocessors, Interconnection Structures, Interprocessor Arbitration. Interprocessor Communication and Synchronization, Cache Coherence.

TEXT BOOKS:

1. Computer System Architecture – M.Moris Mano, IIIrd Edition, PHI / Pearson, 2006.
2. Computer Organization – Car Hamacher, ZvonksVranesic, SafwatZaky, V Edition, McGraw Hill, 2002.

REFERENCE BOOKS:

1. Computer Organization and Architecture – William Stallings Seventh Edition, PHI/Pearson, 2006.
2. Computer Architecture and Organization – John P. Hayes, Mc Graw Hill International editions, 1998.